IN THE UNITED STATES
PATENT AND TRADEMARK OFFICE

Applicant:	Avery, et al.	Case: SAR 14179	
Serial No.:	10/077,833	Filed: November 5, 2001	OFFICIAL
Examiner:	Tran, Tan N.	Group Art Unit: 2828	

Title: **SILICON CONTROLLED RECTIFIER ELECTROSTATIC DISCHARGE PROTECTION DEVICE WITH EXTERNAL ON-CHIP TRIGGERING AND COMPACT INTERNAL DIMENSIONS FOR FAST TRIGGERING**

COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, VA 22313-1450

SIR:

DECLARATION UNDER 37 C.F.R. § 1.131

We, Leslie R. Avery, John Armer, and Koen G. M. Verhaege, hereby declare as follows:

1. That we are the inventors of the above-captioned patent application who are presently available to execute this declaration; and that inventors Christian C. Russ and Markus P. J. Mergens have moved to Germany and are not available to execute this declaration;

2. That we are inventors of the subject matter described and claimed in the present application and are familiar with the disclosure and pending claims, and that the disclosure of the present application describes an invention that was conceived prior to October 10, 2001;

3. That rejected claims 1-23 define embodiments that were conceived prior to October 10, 2001, and constructively reduced to practice by describing the embodiments in the present patent application filed November 5, 2001, as evidenced by Exhibits A-E;

4. That the subject matter of claims 1-23 was diligently pursued by Applicants from a time beginning before October 10, 2001, until filing of the present patent application on November 5, 2001, or any earlier actual reduction to practice;

5. Exhibits A through E are enclosed herewith in support of declaration that we conceived of and reduced to practice the present invention in this country on

37 C.F.R §1.131 Declaration
Serial Number: 10/077,833

or before the publication date of the U.S. patent publication U.S. 2002/0041007 A1 by "Russ", filed October 10, 2001 and published April 11, 2002 ;

6. Exhibit A is a copy of a test data sheet including test structure analysis data for a grounded-gate silicon controlled rectifier (GGSCR) of the present invention;

7. Exhibit B is a copy of page 11 from a document entitled "TBS CMSO2 RF ESD test chip" describing various GGSCR structures of the present invention on a test chip;

8. Exhibit C is a copy of page 13 from the document entitled "TBS CMSO2 RF ESD test chip" depicting a layout example of the GGSCR of the present invention, where the GGSCR includes an external trigger GGNMOS device coupled to an SCR of the present invention.

9. Exhibit D is a copy of page 24 from a document entitled "C10N 2kV ESD design Guidelines, Bus Concepts, and Circuits" depicting various schematics of the GGSCR structures of the present invention for different supply voltage environments;

10. Exhibit E is a copy of page 25 from the document entitled "C10N 2kV ESD design Guidelines, Bus Concepts, and Circuits" depicting a cross-sectional view and layout details of the GGSCR having an external, on-chip, trigger GGNMOS coupled to the SCR of the present invention; and

11. That the disclosures of Exhibits A-E are dated prior to October 10, 2001.

The undersigned, Leslie R. Avery, John Armer, and Koen G. M. Verhaege, hereby declare that all statements made herein of our own knowledge are true and that these statements made on information and belief are believed to be true and further that these statements were made with knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of this application or any patent resulting therefrom.

July 29, 2003 Leslie Ronald Avery
Date Leslie R. Avery

7-28-2003 John Armer
Date John Armer

8-20-2003 Koen G. M. Verhaege
Date Koen G. M. Verhaege

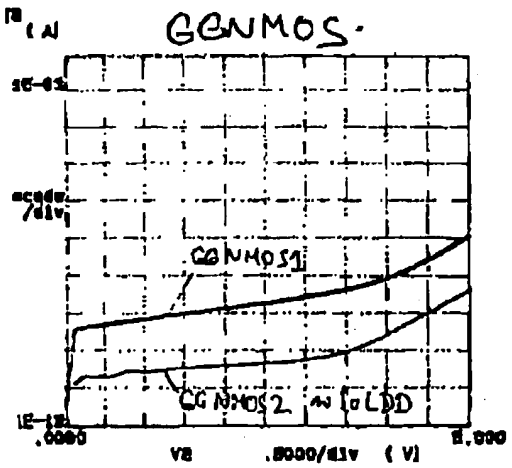
H7L7 MOSART2

T1 (=NOSG)

all Vs GND (p.20)

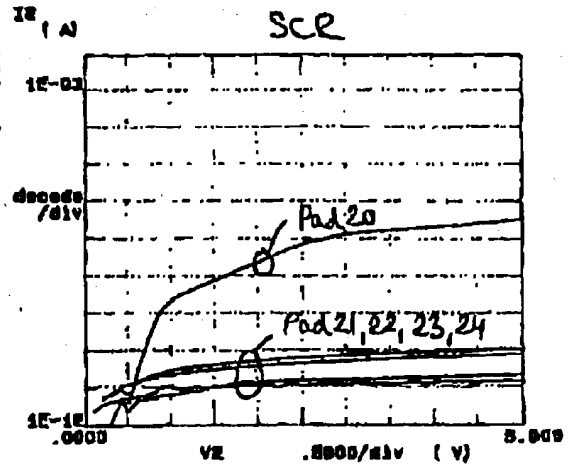
EXHIBIT A

GGNMOS

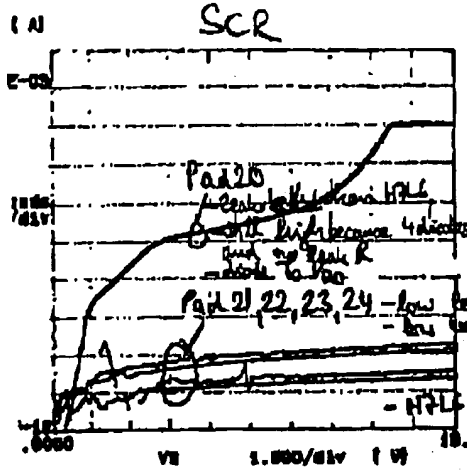


no major change to H7L6 (all okay)

SCR



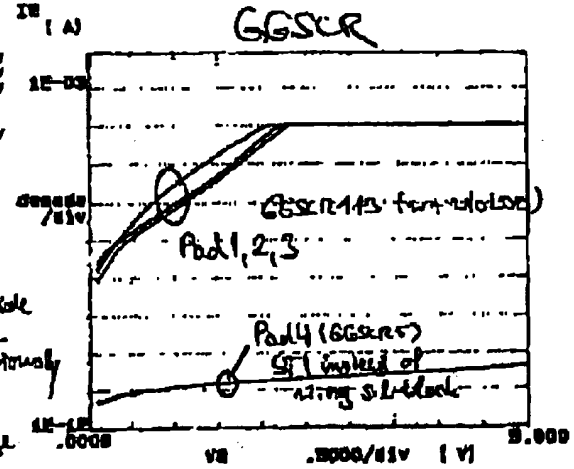
SCR



Pad20: 4x darlington: leakage reduced but still high

Pad21-24 all good

GGSCR



exactly same as T2 (SG)

completely the same as on H7L6 probably due to first n-well-p-well diode

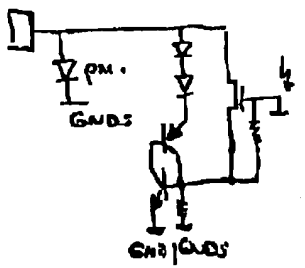
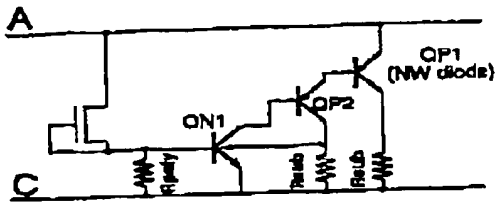
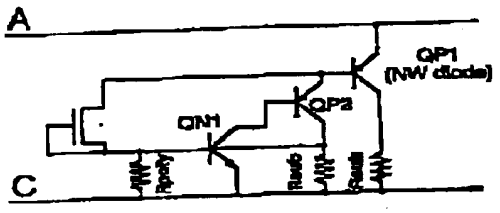


EXHIBIT B

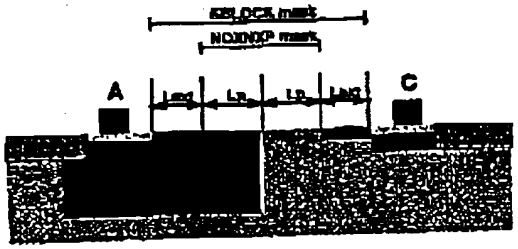
GGSCR Structures



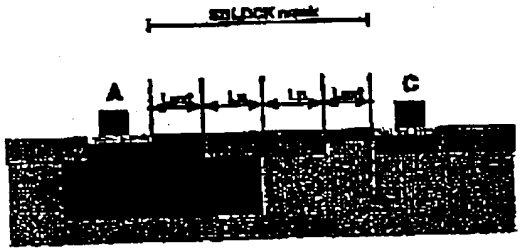
GGSCR with direct triggering (NMOS connected before diode-QP1) – Type A



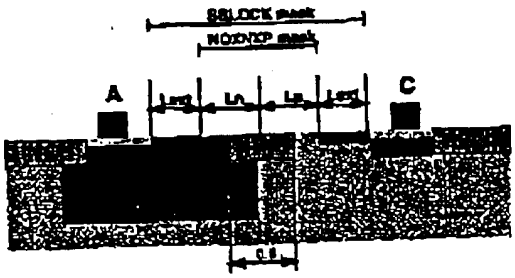
SCR with indirect triggering (NMOS connected after diode-QP1) – Type B



Standard GGSCR



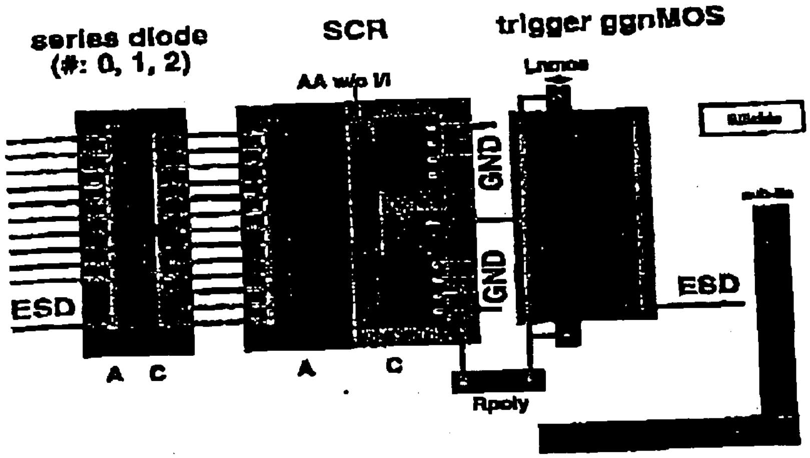
GGSCR with STI and S/D extensions



GGSCR with center STI

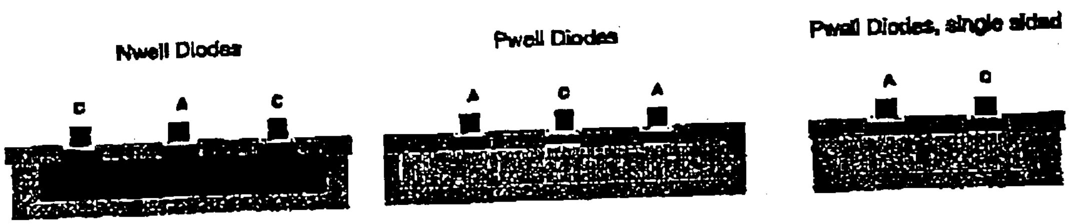
GGSCR with double STI to suppress the S/D extensions

EXHIBIT C



Layout example of GGSCR -- not drawn to scale.

Diodes



Module	Pads: A, C	W (µ)	L(use) (µ)				Remarks	Measurement	Structure Name
0, 51	13, 14	2x20	[illegible]				double sided, NW	TLP, DC [illegible]	[illegible]
[illegible]	15, 16	2x20	[illegible]				double sided, PW	TLP, DC [illegible]	[illegible]
[illegible]	17, 18	[illegible]	[illegible]				[illegible], used for back-to-back	TLP, DC [illegible]	[illegible]
[illegible]		4	[illegible]				double sided, NW	TLP, DC [illegible]	only in S-parameter field
[illegible]		4	[illegible]				double sided, PW	TLP, DC [illegible]	only in S-parameter field
[illegible]		[illegible]	[illegible]				single sided, as in GGSCR	TLP, DC [illegible]	only in S-parameter field

S-Parameter Calibration Structures

Module									Structure Name
[illegible]	open								only in S-parameter field
[illegible]	short								only in S-parameter field

EXHIBIT D

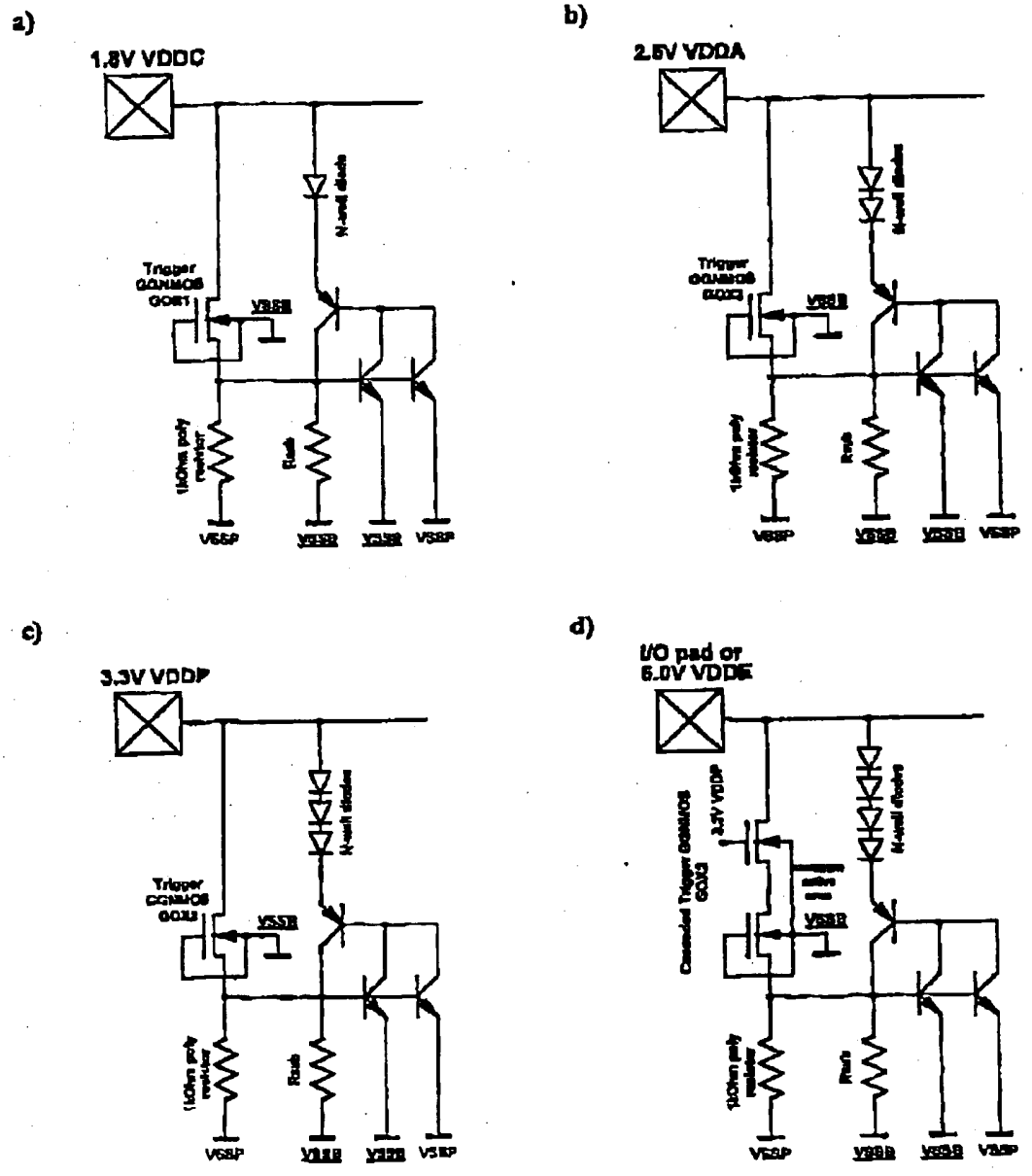


Figure 11 Schematics of the GGSCR for the different supply voltage environments. Note the split NPN transistor of the SCR to accommodate ESD stress for both cases, versus VSSP (noisy source bus) and versus VSSB (quiet substrate bus).

EXHIBIT E

Design rules SCR:

- W ≥ 50um (minimum requirement would be 35um but there needs to be a margin that includes voltage drops due to bus resistance such that the maximum voltage drop stays within the ESD design window)
- spacing from contact to silicide edge = 0.6um
- spacing from silicide edge to diffusion edge = 0.6um
- no-implant/no-STI-region: requires a special CAD layer operation - only the well implants are present
- spacing from diffusion edge to well-to-well junction (i.e. the no-implant/no-STI-region) = 0.9um
- NPN-emitter and trigger taps intermittent (3 segments for a 50-um-wide SCR with 2 trigger taps, no trigger taps at device extremities), local substrate connections not adjacent to trigger taps but shifted

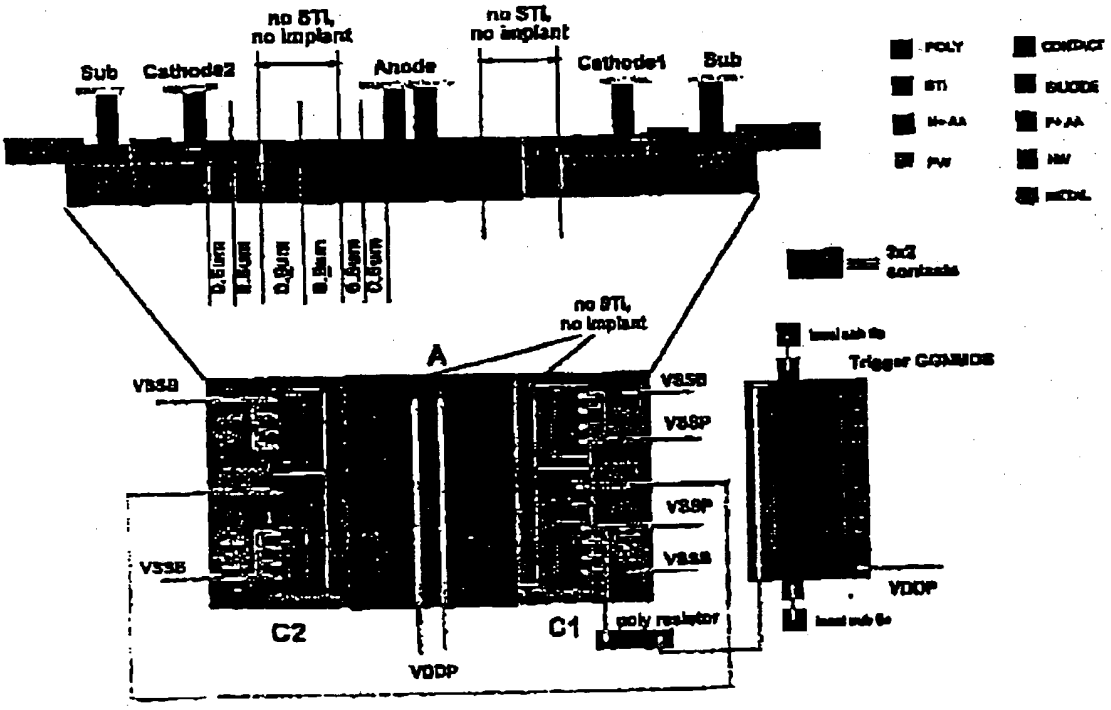


Figure 12 Cross-sectional view and layout details of the GGSCR.